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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,556	12/03/2003	Pei-Ren Jeng	COR 135	4023

7590 09/23/2004

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EXAMINER	
CHEN, JACK S J	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,556	JENG ET AL.	
	Examiner	Art Unit	
	Jack Chen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 03 December 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

In response to the communication filed on December 3, 2003, claims 1-9 are active in this application.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Oath/Declaration

Oath/Declaration filed on December 3, 2003 has been considered.

Drawings

3. Figure 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings

are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 4-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Liaw, U.S./6,448,140 B1.

Liaw discloses a method for forming a semiconductor device, which comprises forming a gate stack including a metal silicide 4 on a tunnel oxide layer 2 (fig. 1); forming a drain and source regions 6 (fig. 1) with said gate stack as a mask; etching a sidewall of said metal silicide (fig. 3); performing an annealing process in an oxygen-steam ambient (col. 5, lines 4-10; fig. 4); and forming a spacer 9c/10 (fig. 5) for said gate stack; see figs. 1-7; cols. 1-10 for more details.

Re claim 5, wherein said etching a sidewall of said metal silicide comprises applying a solution having a high etch selectivity to said metal silicide (fig. 3; col. 4, line 55 to col. 5, line 3).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-3 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art or Woo et al., U.S./5,210,047 taken with Liaw, U.S./6,448,140 B1 and further in view of Huang et al., U.S. Pub. No. 2003/0181007 A1.

Applicant's admitted prior art discloses a method for forming a semiconductor device, which comprises depositing a first polysilicon layer 16, ONO layer 18, second polysilicon layer 20, a tungsten silicide 22 and a hard mask layer 24 over a tunnel oxide layer 14 for a gate structure having a sidewall (fig. 1); forming a drain and source regions 30/32 with said gate

structure as a mask; performing an annealing process and forming a spacer 28 on said sidewall. See fig. 1, pages 1-3 for more details.

Woo et al. also discloses a method for forming a semiconductor device, which comprises depositing a first polysilicon layer 21, ONO layer 24, second polysilicon layer 22, a tungsten silicide 32 and a hard mask layer 33 over a tunnel oxide layer 29 for a gate structure having a sidewall (figs. 3-4); forming a drain and source regions 38/39/40 with said gate structure as a mask; performing an annealing process (col. 7, lines 10-55) and forming a spacer 48 (fig. 6) on said sidewall. See figs. 1-11; cols. 1-12 for more details.

Applicant's admitted prior art and Woo et al. disclosed above; however, they are silent to cleaning the tungsten silicide with a solution having a high etch selectivity to the tungsten silicide.

Liaw teaches a method for forming a semiconductor device, which comprises forming a gate stack including a metal silicide 4 on a tunnel oxide layer 2 (fig. 1); forming a drain and source regions 6 (fig. 1) with said gate stack as a mask; *etching/cleaning a sidewall of the tungsten silicide using a solution having a high etch selectivity to metal silicide (fig. 3; col. 4, line 55 to col. 5, line 3)*; performing an annealing process in an oxygen-steam (oxygen free radicals) ambient (col. 5, lines 4-10; fig. 4); and forming a spacer 9c/10 (fig. 5) for said gate stack; see figs. 1-7; cols. 1-10 for more details.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further forming the recess in the tungsten silicide as taught by Liaw in the method of applicant's admitted prior art or Woo et al. in order to improve the performance of the memory device (i.e., preventing the leakage current from the

tungsten silicide layer; accommodate the unequal growth of the silicon oxide during the oxidation step, etc.).

The further difference between the instant claimed invention and the above prior art is as following: using hydrogen and oxygen gases for the rapid thermal treatment.

It is well known in the art to use wet or dry oxidation method through rapid thermal treatment, such will lower the thermal budget. For example, Huang et al. teach a method for forming a semiconductor device, which includes using hydrogen and oxygen gases (at 10.5 Torr) for the rapid thermal treatment (0023), see figs. 1-11 and page 1-3 for more details.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to using hydrogen and oxygen gases for the rapid thermal treatment as taught by Huang et al. in the method of applicant's admitted prior art (Woo et al.) and Liaw in order to lower the thermal budget.

10. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woo et al., U.S./5,210,047 taken with Choi et al., U.S./6,740,550 B2 and further in view of Huang et al., U.S. Pub. No. 2003/0181007 A1.

Woo et al. also discloses a method for forming a semiconductor device, which comprises depositing a first polysilicon layer 21, ONO layer 24, second polysilicon layer 22, a tungsten silicide 32 and a hard mask layer 33 over a tunnel oxide layer 29 for a gate structure having a sidewall (figs. 3-4); forming a drain and source regions 38/39/40 with said gate structure as a mask; performing an annealing process (col. 7, lines 10-55) and forming a spacer 48 (fig. 6) on said sidewall. See figs. 1-11; cols. 1-12 for more details.

Woo et al. disclosed above; however, Woo et al. is silent to cleaning the tungsten silicide with a solution having a high etch selectivity to the tungsten silicide.

Choi teaches a method for forming a semiconductor device, which comprises cleaning the tungsten silicide with a solution having a high etch selectivity to the tungsten silicide (fig. 5; col. 8, lines 28 to col. 9, line 25). See figs. 1-15C and cols. 1-22 for more details.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further forming the recess in the tungsten silicide as taught by Choi in the method of Woo et al. in order to improve the performance of the memory device (i.e., preventing the leakage current from the tungsten silicide layer; accommodate the unequal growth of the silicon oxide during the oxidation step, etc.).

The further difference between the instant claimed invention and the above prior art is as following: using hydrogen and oxygen gases for the rapid thermal treatment.

It is well known in the art to use wet or dry oxidation method through rapid thermal treatment, such will lower the thermal budget. For example, Huang et al. teach a method for forming a semiconductor device, which includes using hydrogen and oxygen gases (at 10.5 Torr) for the rapid thermal treatment (0023), see figs. 1-11 and page 1-3 for more details.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to using hydrogen and oxygen gases for the rapid thermal treatment as taught by Huang et al. in the method of Woo et al. and Choi et al. in order to lower the thermal budget.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gilton et al., U.S./6,143,611 teach the similar processes for forming the device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (9:00am-6:30pm) alternate Monday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jack Chen
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Art Unit 2813